

Notice of References Cited	Application/Control No. 09/843,573	Applicant(s)/Patent Under Reexamination DEMLER ET AL.	
	Examiner Thomas H. Stevens	Art Unit 2123	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,345,240	02-2002	Havens, Joseph Harold	703/21
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
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	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
*	U	Lewis et al., "A Prototype Unit for Built-In Self-Test of Analog Circuits" IEEE March 1999. pg. 221-224
	V	Frohlich et al., "A New Approach for Parallel Simulation of VLSI Circuits on a Transistor Level" IEEE 1998 Vol.45. no.6
	W	Orr-S., "Synthesys Tool Enables Mixed-Signal Core Design" EE Times Nov.1999. pg. 1-5.
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.